UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/992,500	11/06/2001	Ravi Kumar DVJ	P04950

CONFIRMATION NO. 6797

FORMALITIES LETTER

OC000000007177592

Docket Clerk
P.O. Drawer 800889
Dallas, TX 75380

Date Mailed: 12/10/2001

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

This application has been accorded an Application Number and Filing Date. The application, however, is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given **TWO MONTHS** from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a)

The required item(s) identified below must be timely submitted to avoid abandonment:

- An Abstract not to exceed 150 words in length, commencing on a separate sheet (37 CFR 1.72(b)).

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

m

15CC

COPY OF PAPERS ORIGINALLY FILED

DOCKET NO. P04950 (NATI15-04950) **PATENT**
Customer No. 23990

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	:	Ravi Kumar DVJ
Serial No.	:	09/992,500
Filed	:	November 6, 2001
For	:	PHASE-LOCKED LOOP FREQUENCY SYNTHESIZER USING AUTOMATIC LOOP CONTROL AND METHOD OF OPERATION
Group No.	:	2817
Examiner	:	(Not Yet Assigned)

Commissioner for Patents
Washington, D.C. 20231

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

Sir:

The undersigned hereby certifies that the following documents:

1. Response to Notice to File Corrected Application Papers;
2. "Replacement" Abstract;
3. Copy of Notice to File Corrected Application Papers; and
4. A postcard receipt;

relating to the above application, were deposited as "First Class Mail" with the United States Postal Service, addressed to Commissioner for Patents, Washington, D.C. 20231, on 2/6/02.

Date: 2/6/02 Kathy Longenecker
Mailer

Date: 6 Feb. 2002 John T. Mockler
John T. Mockler
Reg. No. 39,775

P.O. Drawer 800889
Dallas, Texas 75380
Phone: (214) 922-9221
Fax: (214) 969-7557
E-mail: *jmockler@novakov.com*

DOCKET NO. P04950 (NATI15-04950) **PATENT**
Customer No. 23990

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	:	Ravi Kumar DVJ
Serial No.	:	09/992,500
Filed	:	November 6, 2001
For	:	PHASE-LOCKED LOOP FREQUENCY SYNTHESIZER USING AUTOMATIC LOOP CONTROL AND METHOD OF OPERATION
Group No.	:	2817
Examiner	:	(Not Yet Assigned)

BOX NON-FEE AMENDMENT
Commissioner for Patents
Washington, D. C. 20231

Sir:

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

This responds to the Notice to File Corrected Application Papers dated December 10, 2001, in the above-referenced patent application and has a shortened statutory period of response set to expire on February 10, 2002.

IN THE ABSTRACT

Please revise the Abstract as follows:

A (PLL) frequency synthesizer comprising: 1) a VCO that generates a first clock having frequency, Fout, determined by a loop filter control voltage; 2) a first divider for dividing Fout by N to produce a second clock of frequency, Fout/N; 3) a second divider for dividing a reference frequency, Fin, by M to produce a third clock of frequency, Fin/M; 4) a phase-frequency detector for comparing the second and third clocks, generating an UP signal if the second clock is slower than the third clock, and generating a DOWN signal if the second clock is faster than the third clock; 5) a charge pump that receives the UP and DOWN signals and increases or decreases the control voltage on the loop filter by injecting or draining a charge pump current, Ic; and 6) a loop response control circuit for adjusting Ic as a function of N and M.

SUMMARY

The Applicant respectfully requests reconsideration and allowance of pending claims and that this Application be passed to issue. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *jmockler@novakov.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

NOVAKOV DAVIS & MUNCK, P.C.

Date: 6 Feb. 2002

John T. Mockler
Registration No. 39,775

P.O. Drawer 800889
Dallas, Texas 75380
Phone: (214) 922-9221
Fax: (214) 969-7557
E-mail: *jmockler@novakov.com*

APPENDIX A

ABSTRACT OF THE DISCLOSURE

~~A phase-locked loop (PLL) frequency synthesizer comprising: 1) a voltage controlled oscillator (VCO) that receives a frequency control voltage level stored on a loop filter and generates an output clock signal having an operating frequency, Fout, determined by the frequency control voltage level; 2) a first frequency divider for dividing the operating frequency, Fout, of the output clock signal by a first divider value, N, to produce a first divided clock signal having a frequency, Fout/N; 3) a second frequency divider for dividing a reference frequency, Fin, of an incoming reference clock signal by a second divider value, M, to produce a second divided clock signal having a frequency, Fin/M; and 4) a phase-frequency detector for comparing the first and second divided clock signals and generating an UP control signal if the first divided clock signal is slower than the second divided clock signal and generating a DOWN control signal if the first divided clock signal is faster than the second divided clock signal. The PLL frequency synthesizer further comprises: 5) a charge pump for receiving the UP and DOWN control signals and increasing the frequency control voltage level on the loop filter by injecting a charge pump current, Ic, and decreasing the frequency control voltage level on the loop filter by draining the charge pump current, Ic; and 6) a loop response control circuit for adjusting a value of Ic as a function of the first divider value, N, and the second divider value, M.]~~ A (PLL) frequency synthesizer comprising: 1) a VCO that generates a first clock having frequency, Fout, determined by a loop filter control voltage; 2) a first divider for

dividing Fout by N to produce a second clock of frequency, Fout/N; 3) a second divider for dividing a reference frequency, Fin, by M to produce a third clock of frequency, Fin/M; 4) a phase-frequency detector for comparing the second and third clocks, generating an UP signal if the second clock is slower than the third clock, and generating a DOWN signal if the second clock is faster than the third clock; 5) a charge pump that receives the UP and DOWN signals and increases or decreases the control voltage on the loop filter by injecting or draining a charge pump current, Ic; and 6) a loop response control circuit for adjusting Ic as a function of N and M.